Real-Time & Multi-Core
the upcoming migration

benefits

- reduced power and cooling
- reduced space and weight
- increased computation
...and more

industry has a large body of certified single-core hard real-time software

old software migrated en-masse, new software developed to use extra CPU

this is not risk-free
Single-Core Equivalence

practical multi-core migration
sce

single-core equivalence

is

a framework of OS-level techniques
implementable on commercial MCP platforms
for strict partitioning of shared resources
so that each core can be treated as a single-core chip
from a schedulability analysis
and certification perspective
$m$ Application Cores
+ 1 I/O Core

Per-Core Assigned Cache

Shared Interconnect

Per-Core Assigned Memory Bandwidth

Per-Core Private DRAM Banks

SCEx single-core equivalence is

Colored Lockdown (RTAS)

MemGuard (RTAS)

Palloc (RTAS)
sce
single-core equivalence
is
Colored Lockdown
[RTAS'13]
MemGuard
[RTAS'13]
Palloc
[RTAS'14]
Modular Certification

*certify core-by-core, up to m*

- WCET(1)
  
  Certification almost identical to single-core case

- WCET(m)
  
  Certification done for m or **less** active cores
SCE Methodology

*a step-by-step design*

1. Consider multi-core platform
2. Determine relevant parameters
3. Profile workload and define partitions
4. Collect experimental measurements
5. Compute WCET\((m)\)
6. Check per-partition schedulability
7. TEST & PRODUCTION
SCE Methodology

*a step-by-step design*

**Requirement for COTS**
- MMU unit, virtual memory
- Cache locking, by-wayby-line
- Known physical-to-DRAM mapping
- Per-core performance monitoring

**Consider multi-core platform** → **Determine relevant parameters** → **Profile workload and define partitions**

**Collect experimental measurements** → **Compute WCET(m)** → **Check per-partition schedulability**

**For each application**
- Device a ordered list of hot memory pages
- Assign application to partition and partition to core

**TEST & PRODUCTION**
Requirement for COTS

- **MMU unit**, virtual memory
- **Cache locking**, by-way/by-line
- Known **physical-to-DRAM mapping**
- Per-core **performance monitoring**
For each application

- derive a **ordered** list of **hot memory** pages
- assign application to **partition** and partition to **core**
No matter what is the pick of \( m \), measurements always done in isolation.

Construct

*Progressive Lockdown Curve*

**Progressive Lockdown Curve for Tracking Benchmark**

\[ \mu_i = \text{leftover number of misses} \]

\[ \text{WCET}(I) = C_i \]
Progressive Lockdown Curve

Progressive Lockdown Curve for Tracking Benchmark

- Progressive Lockdown Curve
- WCET using entire L3

$\mu_i = \text{leftover number of misses}$

$\text{WCET}(1) = C_i$
Compute WCET(m)
WCET\( (m) \) Calculation

accounting for resource partitioning

\[ WCET(1) = C_i \]
\[ \mu_i = \text{residual misses} \]

\[ WCET(m)_i = C_i + \mu_i \cdot L_{size} \left( \frac{m}{BW_{\text{min}}} - \frac{1}{BW_{\text{max}}} \right) \]
Response Time

\[
R_i(k + 1) = WCET(m)_i + \sum_{\tau_j \in hp(i)} \left[ \frac{R_i(k)}{T_j} \right] WCET(m)_j + B_{MG}
\]

\[C_i + \mu_i \cdot L_{size} \left( \frac{m}{BW_{min}} - \frac{1}{BW_{max}} \right) \]
SCE Validation
using COTS hardware

8 cores

PMU

MMU

P4080

atomic locking
SCE Validation

$WCET(m)\ bound$
WCET($m=8$) for Tracking Benchmark

- Progressive Lockdown Curve
WCET\((m=8)\) for Tracking Benchmark

- Progressive Lockdown Curve
- Measured WCET with \(m\) active cores and SCE
$\text{WCET}(m=8)$ for Tracking Benchmark

- Progressive Lockdown Curve
- Measured WCET with $m$ active cores and SCE
- $\text{WCET}(m) = C'_{\text{sce}}$ from analysis
SCE Validation

$WCET(m)$ sensitivity

$WCET(m)_i$

$C_i + \mu_i \cdot L_{size} \left( \frac{m}{BW_{min}} - \frac{1}{BW_{max}} \right)$
SCE Validation

WCET(m) sensitivity

\[ WCET(m)_i \]

\[ C_i + \mu_i \cdot L_{\text{size}} \left( \frac{m}{BW_{\text{min}}} - \frac{1}{BW_{\text{max}}} \right) \]
SCE Validation

$WCET(m) \text{ sensitivity}$

$WCET(m)_i$

$C_i + \mu_i \cdot L_{size} \left( \frac{m}{BW_{min}} \right)$
Sensitivity to $BW_{max}$ parameter

$C_{sce}$ with $BW_{max} = 2.5$ GB/s

Time (ms)

Number of allocated pages
Sensitivity to $BW_{\text{max}}$ parameter

- $C_{\text{sce}}$ with $BW_{\text{max}} = 2.5 \text{ GB/s}$
- $C_{\text{sce}}$ with $BW_{\text{max}} = 1000 \text{ GB/s}$

Time (ms)

Number of allocated pages
Select $m$, SCE provides a constant $\text{WCET}(m)$

Resource partitioning at OS-level, use on COTS

Reuse single-core software & practices
Thanks.