

Ying Ye

111 Cummington Mall, RM 138
Boston, MA 02215

yingy@bu.edu
(857) 272-2053

PROFILE OS/hypervisor kernel developer, real-time system researcher
Experienced C/C++ programmer

EDUCATION **Boston University**, Boston, MA GPA: 3.72 / 4
PhD candidate in Computer Science (September 2011 - August 2017)
Advisor: Richard West

Tongji University, Shanghai, China GPA: 4.41 / 5
Bachelor of Computer Science (June 2011)
Shanghai Excellent Graduate

WORK EXPERIENCE **VMware Inc.**, Palo Alto, CA (Summer 2016)
Software Engineer Intern
Joined VMware **ESXi hypervisor** resource management team. Investigated Intel processor's new cache partitioning feature and implemented a cache management logic inside hypervisor kernel. Result showed reduced cache contention for virtual machines with low latency requirement, thus improving system's quality of service.

Cisco Systems Inc., Cambridge, MA (Summer 2015)
Software Engineer Intern
Worked in a 20+ **agile** development team building web-based application that manages Cisco security devices (routers and firewalls). Contributed most to the backend server based on Java Spring Framework. Heavily involved in the whole scrum process with weekly sprint.

RESEARCH PROJECT **Multicore Real-Time Operating System for Autonomous Driving**
(September 2016 – April 2017)
Implemented a real-time **virtualization** system based on the separation kernel design. The solution allows a general purpose OS (Linux) to be running inside a VM while still being controlled by a real-time OS in another VM. Experiment demonstrated that, while running a machine-learning-based image classification program side by side with an object avoidance task, the real-time properties of the latter remained unaffected.

Predictable Resource-aware Multicore Scheduling
(September 2014 – May 2016)
Designed a real-time multicore scheduling algorithm and load balancing framework to address contention on shared caches and memory buses, while improving CPU utilization. Proposed a memory-aware scheduling policy with novel performance metric, which outperformed existing metric. Experiment showed that our system's

real-time properties were greatly enhanced.

Performance Isolation via Software Cache Partitioning

(January 2013 - February 2014)

Proposed a **memory management** framework in **Linux kernel** that partitions shared hardware cache on multicore through the use of dynamic page coloring, providing performance isolation amongst applications. Experiments showed a noticeable reduction in program performance variation up to **39%**, in the presence of heavy contention from co-runners.

SKILLS

C/C++, Java, OpenMP, Shell Script, Python, ANTLR, ZigBee, Sensors

AWARDS

RTSS 2016 Student Travel Grant	(Fall 2016)
Intel Modern Code Developer Challenge: Trailblazer (\$500)	(Fall 2015)
PACT 2014 Student Travel Grant	(Summer 2014)
CPS Week 2014 Student Travel Grant	(Spring 2014)
Champion of Chinese Collegiate National Climbing	(Summer 2011)

PUBLICATIONS

MARACAS: A Real-Time Multicore VCPU Scheduling Framework

Ying Ye, Richard West, Jingyi Zhang, Zhuoqun Cheng, in Proceedings of the 37th IEEE Real-Time Systems Symposium (RTSS'16).

COLORIS: A Dynamic Cache Partitioning System Using Page Coloring

Ying Ye, Richard West, Zhuoqun Cheng, Ye Li, in Proceedings of the 23rd International Conference on Parallel Architectures and Compilation Techniques (PACT'14).

Building Real-Time Embedded Applications on QduinoMC: A Web-connected 3D Printer Case Study

Zhuoqun Cheng, Richard West, **Ying Ye**, in Proceedings of the 23rd IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'17) (**Best Student Paper**).

ACTIVITIES

Volunteer of World Expo 2010 (Spring 2010)